Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HEDLEY DAVIS

Appeal No. 1998-2189
Application 08/097,372[1]

ON BRIEF

Before THOMAS, BARRETT, and LEVY, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

[1] Application for patent filed July 23, 1993, entitled (as amended in Paper No. 6) "Bidirectional Data Transfer Protocol Primarily Controlled By A Peripheral Device."

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-10 and 13. Claims 11 and 12 are canceled.

We reverse.

BACKGROUND

The disclosed invention relates to a bidirectional communications method and system for transferring a plurality of data values between a first processor and a second processor. The first processor exclusively controls a direction signal and an asynchronous clock signal to transfer data, which is said to provide a simpler communications interface and protocol.

Claim 1 is reproduced below.

> 1. A bidirectional communications system for transferring a plurality of data values between a first processor means and a second processor means, each data value representing a respective plurality of data bits, the system comprising:
>
> direction control means for forming and transmitting a direction signal from the first processor means to the second processor means, to enable the second processor means to transfer data to the first processor means when the direction signal has a first state, and to notify the second processor means that the first processor means is ready to transfer data to the second processor means when the direction signal has a second state, said direction signal being exclusively driven by the first processor means;

> data transfer control means for forming and transmitting a clock signal from the first processor means to the second processor means, the data transfer control means including means for asynchronously changing the clock signal from a first state to a second state when each bit of a respective one of the plurality of data values is transferred, and for resetting the clock signal to the first state after each individual bit of a data value is transferred, said clock signal being exclusively driven by the first processor means; and
>
> data transfer means responsive to the direction signal and the clock signal for transmitting the plurality of data values between the processors as indicated by the direction signal.

The Examiner relies on the following references:

Costes et al. (Costes)	4,999,769	March 12, 1991
Bush et al. (Bush)	5,150,465	September 22, 1992

Claims 1-10 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bush and Costes.

We refer to the final rejection (Paper No. 8), the examiner's answer (Paper No. 16) (pages referred to as "EA__"), and the supplemental examiner's answer (Paper No. 18) (pages referred to as "SEA__") for a statement of the Examiner's position, and to the brief (Paper No. 14) (pages referred to as "Br__") and the reply brief (Paper No. 17) (pages referred to as "RBr__") for a statement of Appellant's arguments thereagainst.

OPINION

Grouping of claims

The Examiner errs in stating that the brief fails to separately argue the claims and that, therefore, the claims stand or fall together (EA2). Appellant's brief clearly argues four separate groupings of claims, as discussed in Appellants' reply brief (RBr1-4). Since the rejection addresses all the claims, the Examiner's statement is harmless error and it is not necessary to remand the case to the Examiner.

Obviousness

Appellant argues that the combination of Bush and Costes does not disclose the limitations of "said direction signal being exclusively driven by the first processor means" and "said clock signal being exclusively driven by the first processor means," and does provide any motivation for the combination.

Direction signal

The Examiner seems to find the "first processor means" to be the CPU 12 in Bush and, by default, the "second processor

means" to be the microprocessor 34 in the I/O controller 24 of drive 20 (figures 1 and 2). The Examiner finds that Bush teaches (EA4):

> direction control means for forming and transmitting a direction signal from the first processor to the second processor (Abstract; Fig. 2; col. 11, lines 17 - 31);
>
> . . .
>
> Bush clearly discloses a direction signal exclusively driven by a first processor (processor 12). Specifically, Bush teaches information that includes details of the direction of transfer (from host to peripheral or from peripheral to host) wherein the disk driving software executed, on the processor, writes "set up information into appropriate registers 40" (col. 9, lines 13 - 18, 29 - 44).

We find the Examiner's reasoning inconsistent because column 11 and column 9 refer to different transfer modes where the direction is specified by different processors. Column 9 refers to a block-transfer compatible drive operation, whereas column 11 refers to the "flex mode" drive operation, which can emulate a variety of different block transfer protocols. Although the Examiner's explanation is not specific, we agree with Appellant's interpretation (Br6) of the rejection referring to column 11 as referring to Bush's DTH (direction to host) bit, register R2, bit 3, described at column 11, lines 26-30, and possibly also the DRQ (data request bit),

register R2, bit 4, described at column 11, lines 17-25. According to the flex mode description, when written by the drive 20, registers R2 and R3 contain the least-significant byte (LSB) and most-significant byte (MSB), respectively, of a 16-bit Operation Status Word (col. 10, lines 59-63). After registers R2 and R3 are written, an interrupt to the host adapter 32 is initiated to notify the host, processor 12, that the status has been updated (col. 11, lines 2-5). Thus, the DTH and DRQ bits are written by the drive 20 and read by the processor 12 (Table 3, col. 24); accordingly, processor 34 must be the first processor means and processor 12 must be the second processor means to be consistent with claim 1. Column 9 describes a block transfer mode where information, including the direction of transfer, is written by disk driving routines on the processor 12 to be read by the controller 24 (col. 9, lines 31-56). Thus, processor 12 must be the first processor means and processor 34 must be the second processor means to be consistent with claim 1. For the purpose of discussion, we use the disclosure at column 11.

The DTH and DRQ bits in register R2 are written by only drive 20 containing the first processor means 34. Appellant's

argument (Br6) that the contents of the DRQ bit, bit 4, are not exclusively driven by the first processor 34 because bit 4 is also set by processor 12, referring to column 12, lines 10-13 and 37-44, is in error. It is true that registers R1-R10 are written to by both drive 20 and processor 12 as shown in Table 3 (col. 24), where the middle column indicates the meaning attached to the register when written by drive 20 and read by processor 12, and the third column indicates the meaning attached to the registers when written by processor 12 and read by controller 24 containing processor 34. However, although both processor 12 and processor 34 write to the same register, the registers have different meanings depending on which processor does the writing. The status bits DRQ (bit 4) and DTH (bit 3) in register R2 are written only by drive 20; when bits 3 and 4 are written by processor 12, they have different meanings (col. 12, lines 37-45, line 55 (bit 3 is unused); figure 4c). Thus, we find that processor 12 does not write a direction signal.

Appellant's argument (RBr5) that two different processors 12 and 34 control the direction to host bit DTH (RBr5) is apparently based on the Examiner's finding in the examiner's

answer that processor 12 is the first processor that controls the direction of data transfer and the fact that register R2 is written by the disk drive 20. As noted in the preceding paragraph, processor 12 does not write bits DTH or DRQ in the flex mode of column 11.

For the reasons discussed in the preceding two paragraphs, we find that Bush teaches "said direction signal being exclusively driven by the first processor means."

Appellant has argued only the limitation of "said direction signal being exclusively driven by the first processor means" in connection with the "direction control means." Nevertheless, we note that the Examiner's rejection does not address or evidence any recognition of the other limitations of the "direction control means." The limitation of the "direction signal from the first processor means to the second processor means, to enable the second processor means to transfer data to the first processor means when the direction signal has a first state" could be considered to be broadly met since the second processor 12 is broadly "enabled" to transfer data to the first processor 34 (in the controller 24) when the DTH bit is reset. However, the

limitation of "[the direction signal] to notify the second processor means that the first processor means is ready to transfer data to the second processor means when the direction signal has a second state" is more problematic. After the registers R2 and R3 are written by the drive 20, an interrupt to the host adapter 32 is initiated to notify the host processor 12 that the status has been updated (col. 11, lines 2-5). Thus, it appears that the DTH direction bit in Bush does not perform the recited function of notifying the second processor means 12. However, since the limitations are not argued, we do not rely on them. See 37 CFR § 1.192(c)(8)(iv) (1995).

Clock signal

The Examiner finds that "Bush does not explicitly teach exclusively driven clock signals" (EA4). This statement is misleading in that "does not explicitly teach" (emphasis added) suggests that the teaching might be implicit, when, in fact, Bush is silent about clock signals. The Examiner finds that Costes discloses a clock signal 28 exclusively driven by the DMA controller 12, citing column 3, lines 44-53 (EA4-5;

SEA2). Appellant's note that this is a new point of argument raised for the first time in the examiner's answer (RBr5).

We agree with Appellant's description of Costes (RBr6). In Costes, a DMA controller synchro clock signal on line 28 is generated by DMA controller 12 and is used by adapter 5 to sample data sent from controller 12 to adapter 5 on the DMA bus (col. 3, lines 44-52). The adapter 5 generates an adapter clock on line 36 which is sent to DMA controller 12 and used to sample the data received from adapter 5 on the DMA bus (col. 3, lines 40-43 and 54-61). We agree with Appellant's finding that "the data transfer means of Costes requires two different clock signals 28 and 36 driven by two different processors 12 and 5, respectively, to transmit the data values between the processors in a direction indicated by the direction signal" (RBr6).

As we understand the Examiner's position, the DMA controller exclusively drives a clock signal because the clock signal on line 36 is generated by inverting the received synchro DMA clock signal on line 28; that is, DMA controller drives both the DMA clock signal 28 and, indirectly, the adapter clock signal 36. We disagree with this reading of the

claim onto Costes, since the two clock signals are not the same clock signal. The description that adapter 5 "generates" adapter clock signal 36 (col. 3, lines 40-43, 51-53), indicates that adapter 5 drives adapter clock signal 36. The DMA clock signal on line 28 is referred to as a "first clock signal" and the adapter clock signal on line 36 is referred to as a "second clock signal" (e.g., col. 1, lines 51-61), indicating two clock signals. On a very elementary level it can be seen that the inverted clock signal on line 36 is not the same signal as the DMA clock signal on line 28 even though it is derived from the signal on line 28. Thus, we agree with Appellant that both processors 12 and 5 drive a separate clock signal. Further, claim 1 requires "said clock signal being exclusively driven by the first processor means" and "data transfer means responsive to the direction signal and the clock signal for transmitting the plurality of data values between the processors as indicated by the direction signal." Claim 1 requires the same clock signal to clock data in both directions, which is not done in Costes (col. 2, lines 4-12). Thus, we find that Costes does not cure the deficiency of Bush with respect to the limitation of "said clock signal being

exclusively driven by the first processor means" and, for this reason, the Examiner has failed to establish a prima facie case of obviousness.

In addition, although not argued, it is not seen how the clock in Costes could possibly teach the other limitations of the "data transfer control means," in particular, "the data transfer control means including means for asynchronously changing the clock signal from a first state to a second state when each bit of a respective one of the plurality of data values is transferred, and for resetting the clock signal to the first state after each individual bit of a data value is transferred." We find no discussion or recognition of these limitations by the Examiner. In Costes, the "clock signal is synchronous with the data sent from the DMA controller" (col. 3, lines 49-50). Thus, the clock signal is not asynchronous as claimed. Furthermore, there is no teaching that the clock should operate to change states, as claimed, to transfer data. It appears that the Examiner has merely tried (unsuccessfully) to find bidirectional data transfer between two processors using a single clock signal and has ignored the functional limitations. Nevertheless, since the limitations

are not argued, we do not rely on them as a basis for our decision. See 37 CFR § 1.192(c)(8)(iv).

Combination

The Examiner concludes that it would have been obvious "to implement clock signals exclusively driven by a processor in Bush because these exclusively driven clock signals are well known in the bidirectional data transfer art, as seen in Costes and therefore represents no patentably distinct feature over the prior art" (EA5).

Assuming, arguendo, that it is true that an exclusively driven clock signals was shown in Costes, the Examiner has not explained how he proposes to modify Bush to incorporate the clock of Costes. Nor do we find any motivation in the references for the (unspecified) modification. The Examiner has merely found a clock and made a conclusory statement that it would have been obvious to combine without providing any logical reasons or analysis. Moreover, as already noted, the Examiner's rejection fails to address most of the functional limitations of the claims and we have no idea how the references could be combined to cure these deficiencies.

Thus, the Examiner has failed to establish a prima facie case of obviousness as to the reasons to combine.

CONCLUSION

Because the Examiner (1) failed to show the limitation of "said clock signal being exclusively driven by the first processor means," and (2) provided no explanation of how Bush and Costes should be combined to produce the claimed subject matter, we conclude that the Examiner has not established a prima facie case of obviousness as to claim 1 and its dependent claims 2-9. Independent claim 10 stands or falls together with claim 1. Independent claim 13 contains a limitation in addition to the limitations of claim 1 and, so, is also patentable over the combination of Bush and Costes. Accordingly, the rejection of claims 1-10 and 13 is reversed.

REVERSED

JAMES D. THOMAS)
Administrative Patent Judge)
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